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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/604,113	06/26/2000	Leland Szewerenko	TI-30126	3785

7590 08/03/2004

ATTEN: ROBERT L. TROIKE
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EXAMINER	
VU, TUAN A	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 08/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/604,113	SZEWERENKO ET AL.	
	Examiner	Art Unit	
	Tuan A Vu	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the Applicant's response filed 5/10/2004.

As indicated in Applicant's response, claims 1-5, 7-9 have been amended. Claims 1-9 are pending in the office action.

Claim Objections

2. Claims 1, 2 are objected to because of the following informalities: the repeated use of 'or' in the claim renders the claim somewhat unclear as to which portions or segments of a long paragraph such 'or' applies to in order to convey a clear understanding of the intended alternative limitation. Suggested is the use of appropriate punctuation to delimit group enclosing each 'or' implication.

Claim 8 is objected because the element 'step' (line 12) should be corrected to be in a plural form.

Claim 9 is objected because it mentions about 'the return' (line 1); this element has not been mentioned explicitly in claim 8; and should be specified further as to indicate which return it pertains to. As it stands, it is interpreted as a return from any call, far or near. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1, 3, 5, and 6 are rejected under 35 U.S.C. 102(a) as being anticipated by Intel, "IA-64 Sotware Conventions and Runtime Architecture Guide", August 1999 (hereinafter Intel).

As per claim 1, Intel discloses method of making a far call or far branch instruction using a near call or near branch instruction that is capable of the transfer of program control a limited distance from address of a near call or branch instruction to a target address comprising the steps of:

determining if a transfer of control is beyond a near call or near branch limitation and if so generating a link time modification of object code by the compiler or assembler by the addition of custom generated object code or trampoline code to the link without changing the compiler generated instructions or expanding compiler generated object code for a long distance transfer of control by redirecting original call to a code which transfer control to the target address (e.g. chp. 8.1; Fig. 8-1; *br.call, displacement ... too large, displacement ... computed at link time, linker ... supply a branch stub* - chp. 8.4.1- Note: the fact that the linker must supply a stub is equivalent to compiler generated instructions are not changed and context is switched to the stub via saving of values at entry point into the stub; and creating a stub when the displacement is found to be large is equivalent to transfer control to the stub a limited distance, thus making it appears like a shorter distance calling).

As per claim 3, Intel discloses a method of making link time far calls or far branches using a near call or near branch instruction that is capable of only the transfer of program control a limited distance from address of a branch instruction to a target address comprising the steps of

determining if a transfer of control is beyond a near call or near branch limitation and if so

generating link time modification of object code by the compiler or assembler by the addition of custom generated object code to the link without changing the compiler generated instructions or expanding compiler generated object code (e.g. Fig. 8-1; *br.call, displacement ... too large, displacement ... computed at link time, linker ... supply a branch stub* - chp. 8.4.1- Note: the fact that the linker must supply a stub is equivalent to compiler generated instructions are not changed and context is switched to the stub via saving of values at entry point into the stub; and creating a stub when the displacement is found to be large is equivalent to transfer control to the stub a limited distance, thus making it appears like a shorter distance calling).

As per claim 5, Intel discloses a method of making a far call or far branch instruction using a near call or near branch instruction that is capable of only the transfer of program control limited distance from address of a branch instruction to a target address comprising the steps of: generating near calls at a compiler or assembler for all external branches or calls; determining if the target address is too distant from a call or branch; and if too far distant generating a trampoline section to the target address and re-directing the near call or branch to the trampoline section ((e.g. Fig. 8-1; *br.call, displacement ... too large, displacement ... computed at link time, linker ... supply a branch stub* - chp. 8.4.1).

As per claim 6, Intel discloses including the step of returning to an original call by returning the control through the trampoline section (e.g. *Procedure exit* - chp. 8.4.1).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2, 4, 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel, "IA-64 Sotware Conventions and Runtime Architecture Guide", August 1999, in view of Mattson, Jr., USPN: 6,317,870 (hereinafter Mattson).

As per claim 2, Intel discloses a method of making a far call or far branch instruction using a near call or near branch instruction that is capable of only the transfer of program control a limited distance from address of a branch instruction to a target address comprising the steps of:

determining if a transfer of control is beyond a near call or near branch limitation and if so

generating a link time modification of object code by the compiler or assembler by the addition of custom generated object code or trampoline code to the link time object code without changing the compiler generated instructions or expanding compiler generated object code for a long distance transfer of control by redirecting original call to a code which transfer control to the target address (Fig. 8-1; *br.call, displacement ... too large, displacement ... computed at link time, linker ... supply a branch stub* - chp. 8.4.1 – see claim 1 Note)

But Intel does not explicitly disclose that if resources are a problem a step of using a sequence of trampolines is further included. The purpose to resolve memory extraneous usage by creating stub code by Intel implies the need to create stubs dynamically by the linker in order to be able to perform a correct link time resolution; and such need entail attempts to create stubs when memory can afford the resource lest more memory resources problem would incur. For a skill in the art, this very purpose of using stub or trampoline code is to dynamically provide a

size-efficient and possibly disposable amount of code without affecting resources of a bigger compilation or execution environment. Mattson, in a method accomplishing link time external resolution using stub import or trampoline similar to Intel's, discloses a known concept that as many stubs as needed to sufficient fulfill the number of external resolution (col. 1, lines 62-67). Hence, in case that Intel does not provide stubs in quantity allowed and dictated by the resources/tasks constraints or demands, it would have been obvious for one of ordinary skill in the art at the time the invention was made to provide additional stubs as the resolution as mentioned above as needed or as resource-permitting as suggested by Mattson because this will provide a very efficient way of resolve linking issues without change to the compiled code and possibly without committing more resources to readjust what has already accomplished prior to the linking resolution step; e.g. performance improvement by Mattson (see Summary of the Invention) or benefits recognized in the use of dynamic stubs in general as mentioned above.

As per claim 4, Intel discloses a method of branch or call instructions comprising the steps of the compiler or assembler generating near-call instructions for all external calls, and near return instructions for all global subroutine returns, ignoring link-time layout of sections; the linker allocating all object code sections, with no need to take into account the limitations of near-branch instructions; for each near external call C, the linker computing the distance from C to its target T and performing the following steps:

determining if the call C and target T are allocated close enough to each other to permit a near call and if so, then call C performs a near call to target T directly with no modification and return to consider the next call; creating trampoline section S1 and modifying call C to point to call B1 in S1 and add any necessary setup code to S1 (e.g. Fig. 8-1; *br.call, displacement ... too*

large, displacement ... computed at link time, linker ... supply a branch stub - chp. 8.4.1 – Note: computing displacement distance for a branch call is equivalent to target T is linkably close enough to permit a near call, with stub a.k.a. trampoline being then effected to enable call restructuring in order to link to target T)

But Intel does not explicitly disclose that if there is already a trampoline S1 to target T that is linkably close enough to call C to permit a near call, then modifying call C to point to call B1 in S1 and returning to consider the next call; nor does Intel disclose continuing with following steps of determining if a second trampoline S2 is needed to reach target T and, if not, then assigning call B1 in S1 to contain a far call to target T, and return to consider the next call; otherwise, determining if a second trampoline S2 already exists to reach target T and if so, then modifying call B1 in S1 to point to existing call B2 in existing S2, and return to consider the next call; otherwise, creating a second trampoline S2 and modifying S1 to perform a far call to call 82 in S2 and add any necessary setup code to S2 and subroutine call 82 in S2 is made to contain a near call to target T and return to consider the next call.

Mattson discloses that a stub is created for use by many callers after the initial caller creates the stub (see Mattson, col. 2, lines 35-45). In view of the rationale as to create as many trampolines or stubs to effect the link time address or external calls resolution as set forth in claim 2, and the implied need to provide efficient linker stubs to enable the far calls resolution as much as required such as taught or suggested by Intel or Mattson, the successive creation of trampoline(s) or stub(s) when it is determined that no trampoline has yet been generated to reach the far call target as described above, or to make use of a existing stub would have been obvious for the same reason as mentioned in claim 2.

As per claim 7, Intel discloses a method of making a far branch or far call instruction using a near branch or near call instruction that is capable of only transferring of program control limited distance from address of a branch instruction to a target address comprising the steps of: computing if the target is too far distant from the near branch or near call limited distance; if it is too far distant then if there is not already a trampoline to the target address then generating a stub or trampoline section to the target address and redirect the near call or near branch to the generated trampoline section (e.g. Fig. 8-1; *br.call, displacement ... too large, displacement ... computed at link time, linker ... supply a branch stub* - chp. 8.4.1).

But Intel does not specify determining if there already is a trampoline and if so redirect the new far call or far branch to that trampoline section. But this limitation of having existing trampolines has been addressed in claim 4 with the rationale using Mattson's teachings.

As per claim 8, Intel discloses a method of making a far call or far branch instruction using a near call or near branch instruction that is capable of only transferring of program control a limited distance from address of a branch instruction to a target address comprising the steps of:

computing if the target address is too far distant from the near branch or near call limited distance; if it is too far distant then generating a trampoline section to the target address and redirect the near call or branch to the generated trampoline section (e.g. Fig. 8-1; *br.call, displacement ... too large, displacement ... computed at link time, linker ... supply a branch stub* - chp. 8.4.1).

But Intel does not explicitly disclose determining if there already is a trampoline section to the target address and if so redirect the new far call or far branch instruction to that trampoline section. But this limitation has been addressed in claim 4 just as it is addressed in claim 7.

Nor does Intel explicitly disclose that if a single trampoline fails to work because of resources, then included are the steps of: generating a second trampoline and generating a far branch or call said first trampoline to the second trampoline section and generating at the second trampoline section a near call or branch to the target address. The limitation as to create additional trampoline or stub sections as long as resources or purposes allowed or required has been addressed in claim 2.

As per claim 9, Intel does not explicitly disclose that return is a near return from the target address to the second trampoline, a far return from the second trampoline and a near return from the first trampoline to the original call. But in view of the creation of stubs in Mattson and the teachings by Intel for returning with restoring state of the caller (re claim 6), this limitation is implicitly disclosed in either Intel or Mattson.

Response to Arguments

7. Applicant's arguments with respect to claims 1-4 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (703)305-7207. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9306 (for formal communications intended for entry)

or: (703) 746-8734 (for informal or draft communications, please consult Examiner before using this number)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA. , 22202. 4th Floor(Receptionist).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAT
July 16, 2004

ANIL KHATRI
PRIMARY EXAMINER